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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Patent Application

Inventor(s): Warren Snyder

Application No.: 09/975,104

Group Art Unit:

Filed: 10/10/01

Examiner:

Title: CAPTURING TEST/EMULATION AND ENABLING REAL-TIME DEBUGGING USING
FPGA FOR IN-CIRCUIT EMULATION

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub- class	Filing Date
T.P.	A	6,460,172	10/01/02	Insenser Farre et al.	716	17	06/21/00

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub- class	Translation	
	B						Yes	No

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	C	
Examiner	Thai Phan	
	Date Considered 2/4/06	

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered.
Include copy of this form with next communication to applicant.